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Production, Characterization and Application of Silicon-on-sapphire Wafers

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Abstract. Silicon-on-sapphire (SOS) thin film systems have had specific electronic applications because they can reduce noise and current leakage in metal oxide semiconductor transistors. However, there are some issues in producing defect-free SOS wafers. Dislocations, misfit, micro twins and residual stresses can emerge during the SOS processing and they will reduce the performance of an SOS product. For some reasons, research publications on SOS in the literature are not extensive, and as a result, the information available in the public domain is fragmentary. This paper aims to review the subject matter in an as complete as possible manner based on the published information about the production, characterization and application of SOS wafers.

Introduction

SOS is a member of the silicon-on-insulator (SOI) family which uses a hetero-epitaxial process to generate thin films of semiconductor materials. When sapphire is used as a substrate, because of its high insulation property and low parasitic capacitance, it can provide lower power consumption, higher frequency and better linearity and isolation than the bulk silicon. Nevertheless, the fabrication process of SOS can introduce defects such as dislocations due to the crystal lattice mismatch between different material layers and because of the difference in thermal expansion coefficients between the grown films and substrates [1]. These can often lead to unusable wafers and increase the cost of production.

This review tends to provide, as complete as possible, some details in terms of the production, defect generation, characterization and application of SOS wafers.

Production

The technology for SOS wafer manufacturing was invented in 1963 in North American Aviation California (now Boeing) as reported by Manasevit and Simpson [2]. Single-crystal deposits of silicon on sapphire crystal were obtained via H_2 reduction of $SiCl_4$ at high temperature. The deposition was on the plane produced by cutting a sapphire rod perpendicular to its fastest growth direction. The quality of the deposited film was found sensitive to the crystal orientation of the substrate. Manasevit also deposited silicon films on spinel and cubic zirconia, but these technologies have never been used in production [3]. Since then many methods have been applied for making SOS thin film systems, such as chemical and physical vapour deposition techniques.

Weisberg et al. [4] used the physical vapour deposition in an oxygen free evaporation system to produce improved crystal. Silicon was sublimed from its solid phase at about 1390°C using an electron bombardment system. The deposition rate achieved was 5 to 7 μm per hour to generate a film thickness of 4 to 20 μm at about 5E-8 Torr. It was found that the use of ultrahigh vacuum (around 2E-9 Torr) does not significantly improve the results in the oxygen-free system. It was concluded that the film deposited on (0001) surface was considerably superior to that on $(1\bar{1}02)$ surface, though without the details of the crystalline defects at the interface. The best crystalline quality was obtained at about 1000°C from the range of 780 to 1000°C. Naber et al. [5] deposited

silicon thin films by the electron beam evaporation in an ultrahigh vacuum on the (0001) and (1$\bar{1}$02) planes of sapphire substrates. They considered different deposition temperatures (500 to 1000°C), different deposition rates (50 to 700Å/min) and different sapphire surface treatments. They found that mechanically polished substrates had poor reproducibility and crystallinity of silicon films at 800 to 1000°C, that single crystal and twinned silicon films would form at 700 to 1000°C on a treated substrate (silicon etched at 1300°C), and that fiber textured films would form at low temperatures between 500 to 700°C. Abrahams et al. [6] used the chemical vapour deposition process to produce SOS wafers to investigate its early growth. The Si layer was grown on the (01$\bar{1}$2) plane at a nominal rate of 0.4 μm/min by the pyrolysis of silane in H_2 at 1000°C. Under a transmission electron microscope, they found microtwins, stacking faults and misorientations in the Si thin films. Inoue et al. [7] deposited silicon films of (100) orientation on (1$\bar{1}$02) sapphire substrates using thermal decomposition of SiH_4 at 950°C with a growth rate of 1.8 μm/min.

Some studies reported that silicon deposition on (0001) sapphire surface would be superior compared to that on its (1$\bar{1}$02) plane [4]. Since the atoms on the (1$\bar{1}$02) plane of sapphire have a similar square symmetry to those on the (100) plane of silicon, this Si plane is used in all CMOS electronics, which enables the SOS technology.

An SOS deposition process is complex and is influenced by many factors. Defects can originate in the vicinity of a silicon-sapphire interface at an early stage of the film growth. Twins and stacking faults can form while small growth centers having four (110) orientations on (1$\bar{1}$02) sapphire substrates coalesce until they are trapped by the surrounding (100) domains [6]. Misfit dislocations also exist in SOS wafers [8]. The formation of the Si layer with small crystallization defects only is extremely difficult as the lattice unconformity between the sapphire substrate and Si thin film is up to 12.5%. This mismatch heteroepitaxy remains as a formidable obstacle in the further development of SOS device products [9].

Recently, some re-growth techniques [8] have been developed to reduce the defects. The first step is to amorpharise a Si thin film by silicon [10] or oxygen [11] ion implantation. Then thermal [10, 11] or laser [12] annealing is used to make the solid phase epitaxial regrowth. The optimum implantation conditions [7] were found to be: (a) the projected range of silicon ions should be around 0.8 times of the Si film thickness, (b) the residual surface crystalline layer should be 0.2 to 0.3 times the deposited Si thickness, and (c) the thermal annealing should be conducted at more than 600°C in N_2 ambient. A higher temperature annealing could lead to more defect reduction [10]. Two-step growth was also applied to reduce the defects in SOS wafers [13], in which a pre-deposited amorphous thin Si layer was used before chemical vapour deposition (CVD). Growing the Si films on sapphire at lower temperatures has been found to be another solution to those problems. Si films can be grown at 650 to 800°C by silicon molecular beam epitaxy (MBE) using an electron gun evaporator. In this case, Si layer coalesced at a thickness of 500 Å and became smooth at 2000 Å [14]. It has been reported that a better silicon thin film can be grown on sapphire substrates at low temperatures by gas-source silicon MBE using disilane (Si_2H_6) [15], although defects do occur. However, no further research or practical applications have been found about this process.

Ultra Thin Si (UTSi®) has been used by Peregrine Semiconductor to improve the quality of the Si thin film on sapphire. This has accelerated commercialization of SOS devices. Processes for 0.50 μm and 0.25 μm thick Si films on sapphire have been developed. The UTSi® technology is very much similar to that of the re-growth method, but the process parameters used in UTSi® to improve the thin film quality have been kept confidential. What can be read from the published information is that the UTSi® technology has made Si films on sapphire substrates with a superior crystallization, even when the film becomes as thin as 100 nm [9]. On the other hand, it has been reported that SOS wafers can also be prepared by a direct wafer bonding method [17], in which a thin silicon wafer is first bonded to a polished sapphire substrate and then is further thinned down to a required thickness (e.g., ≈ 10 μm) by mechanical grinding and chemical etching. It has been claimed that this type of SOS wafers have a better performance compared with the epitaxially grown

ones. However, a performance comparison between a bonded SOS wafer and an UTSi SOS wafer is not available.

Interfacial Defect Detection

To assess the quality and performance of SOS wafers produced, characterization methods and tools are necessary. This section summarizes the following interfacial defect detection techniques including X-ray Laue diffraction, TEM, Ion channeling and X-ray rocking curve.

X-Ray Laue Diffraction. Back to the 1960s, Laue film diffraction image was the most conventional and powerful tool to evaluate the crystalline structure and quality of single crystals. The initial application of this technique in SOS wafers was to examine the quality of silicon films [2]. When the method of silicon deposition under vacuumed was developed, the Laue diffraction (Spot) image was also used to demonstrate the improvement of the thin films [4], which in turn concluded, as discussed previously, that the crystal quality of a thin film on the (0001) plane of sapphire would be better than that on the ($1\bar{1}02$) plane.

Transmission Electron Microscopy (TEM). TEM is the most convincing tool to reveal the details of micro-structural defects from cross-sectional image. The TEM study on SOS wafers was firstly performed by Bicknell [18] who found that the micro-twins and stacking faults were the most common defects. Later on, Abrahams observed misfit dislocations by cross-section TEM along the film growth direction [19]. This was advancement in the evaluation of epitaxial structures. From the dislocation images, it was concluded that the misfit strains in some directions are approximately relieved by misfit dislocations. The TEM technique can monitor the dynamic process of the micro twins at the early stage of SOS growth [6], and can characterize, at the lattice resolution, stacking faults and twins [20]. Based on the observations and images from high resolution TEM, Ponce [21] concluded that the interface is planar and abrupt, and that the interface defects are asymmetric with periodic patterns. The TEM technique has also been applied to measure quantitatively the micro-twin density as a function of the distance from the interface [22]. By examining the differential volume fraction of the micro-twins, it was proved that the strain relief due to micro-twins cannot be greater than 0.7%, indicating that micro-twinning is not the dominant mechanism to release mismatch strains [23]. The main drawbacks of TEM are its destructive nature and complicated sample preparation. These limit its use mainly to laboratory study and make it unsuitable for in-situ quality control.

Ion-Channelling and Rutherford Backscattering. The most attractive feature of ion-channeling is its non-destructive measurement of the distribution and density of imperfections along the depth of a thin epitaxial single-crystal film. The ion-channelling technique has been extensively applied to characterize, monitor and verify the crystal quality after ion-implantation and the subsequent annealing processes in SOS wafers [24]. By applying this method, Picraux [25] observed that the crystal imperfection in a 1μm (001) layer at a certain distance from the interface is greater than that in a 2 μm (111) layer, which suggests that the highest defect density is in the interface and decreases, depending on the film thickness, with the distance away from the interface. However, to conduct a more detailed analysis of different defects, it requires the assistance of other techniques (e.g. TEM) to determine an appropriate dechanneling cross section.

X-ray Topography and X-Ray Rocking Curve Method. Compared with TEM, X-ray transmission topography contrasts provide visualized qualitative information in a nondestructive manner. The X-ray diffraction topography was initially used to study the dislocation density and internal stresses in SOS wafers [26], whose photographic contrasts can show the presence of high density lattice imperfections such as lattice distortion, dislocations and micro twins generated in an SOS wafer during and after a deposition process. Later on, the X-ray rocking curve method was developed as a standard technique [27] to monitor the crystalline quality of SOS wafers produced under different deposition conditions. Trilhe [28] tried to identify the optimum deposition temperature by examining the full width at the half maximum of the X-ray rocking curve with a

dual diffractometer. Rocking curve was applied [29] to investigate the correlation between the crystalline quality and the misorientation angle of the sapphire substrate. The optimum substrate orientation was found to be 2° in a specific direction from (01$\bar{1}$2) plane, in which, the four twin systems are equally active.

Residual Stresses Characterization

A high level of residual stresses can affect the electrical and mechanical properties of a device based on the SOS technology [30]. Curvature method, Raman spectroscopy and XRD stress analyses have been commonly used to measure and characterize residual stresses in SOS wafers.

Curvature Method. This is a conventional tool to investigate stresses in an SOS wafer. Dumin [31] measured the curvature of thick (4 to 20 μm) SOS stripes by Zeiss light section microscope to calculate the residual stresses. It was found that the stress in the film increases with the increase of the film thickness and with the decrease of the sapphire thickness. Ang and Manasevit [30] applied the cantilever beam technique to measure the deflection of a Si film of thickness 1.8 μm on sapphire. The film was deposited by chemical decomposition of silicon tetrachloride vapor in hydrogen at 1150°C, and the compressive stress was calculated as -585 MPa with 20% accuracy.

Raman Scattering. Currently, Raman is one of the dominating tools to measure the film stress in SOS wafers. The technique is straightforward, which can determine the average residual stress in a wafer in a nondestructive manner. Englert [32] employed it to measure the residual stress in the as-grown SOS wafers with films of 0.6 to 0.9 μm in thickness. In his investigation, the anisotropy in the surface was neglected and an equi-axial stress model was assumed in solving the dynamic equations of the cubic lattice. Yamazaki et al. [33] considered the anisotropic thermal expansion coefficients of sapphire and extended the Raman analysis by measuring the polarization characteristics. In their work, stress along depth was investigated by selecting different excitation wavelengths. They noted that the stress is decreasing from the silicon/sapphire interface toward the free surface. The compressive stress at the interface was 600 to 1300 MPa and became 550 to 750 MPa at the surface. Later on, microprobe was employed into the Raman technique to investigate the local stress in SOS wafers with 1 μm resolution [34]. Raman backscattering coupling with Ion-channeling technique was utilized to monitor the stress relaxation and film quality after ion-implanted [35] and laser annealed [36] SOS wafers. The advantage of Raman scattering over the XRD technique, which is to be briefly discussed in the next paragraph, is that it provides a high spatial resolution (1 to 10μm) and high accuracy (±30MPa). However, pre-analyses and assumptions (e.g., biaxial) are required to obtain reliable stress values.

XRD Stress Analysis. This is a popular method to measure strains in crystalline materials in certain lattice [hkl] directions**,** which can then give residual stress estimations (with an accuracy of about 0.01%) from the strains. Vrelland [37] used this technique to calculate the principal strains from the peak shifts of two x-ray rocking curves with reversing diffraction vectors (180° rotation). Carstein [38] investigated film and substrate strain distributions in as-grown Si films of 0.1 and 0.25 μm in thickness with the integration of in-plane and out-of plane geometry in which the in-plane diffraction gives strains ε_{11} and ε_{22} while out of plane geometry defines strain ε_{33}. From these principal strains, strain and stress tensors can be solved by assuming bi-axial stress state. In order to determine a complete stress tensor in an SOS wafer, the measuring directions are limited by the crystallographic orientations of (hkl) planes that contribute to diffraction. Thus 3-axis sample alignments are required to adjust the measured (hkl) plane in the required direction [39]. This normally adds difficulties to the measurement process. Furthermore, to ensure the statistical reliability of an XRD stress analysis, more measuring time is required. This contributes another limitation to analyze ultra-thin SOS (100nm) wafers by this technique.

Having said these, it is clear that TEM is the most effective tool to identify the defect types, but its destructive nature limits the in-situ application of the technique. For an industrial quality control, X-ray topography and rocking curve method shows its advantages because of its fast detection

cycle. Ion-channelling is able to determine the distribution of defects along the depth. However, the defect types should be assumed or pre-determined by other techniques such as TEM. Raman is fast in measuring average stresses with a high spatial resolution. Although the XRD technique is able to reveal a more detailed stress state (e.g., a complete stress tensor), the measuring and calculation process is not very straightforward.

Applications

SOS wafers were primarily used in the areas which require inherent resistance to radiation. Their commercial use to date does not seem to be extensive enough, but growing. A reason of this in the past could be the difficulties in the fabrication of very small SOS transistors for modern high-density applications. Peregrine Semiconductor in the United States succeeded in their practical application of SOS wafers by their customized re-growth technique. The secret of production of efficient the SOS wafers has been very much confined to Peregrine semiconductor itself. Sapphire for SOS based devices was originally located in Australia, but is now moving to Asia as Peregrine is becoming fabless and has inked several agreements with Korean semicon fabs to outsource the production. The business of sapphire material will break the $400M barrier by 2012 with the tremendous growth in SOS devices [40].

SOS devices are mainly used by wireless systems such as radios and military and space structures. The increasing commercialization in these areas demands the production of more of wireless systems which have greater bandwidths and cleaner spectral bands, and smaller, cheaper yet more robust. These require increased system complexity [41].

Summary

There is no doubt that SOS wafers are becoming more and more important to the electronic industries in the fields of wireless communication and radiation hardened components. There are several production processes for as-grown SOS wafers, but accurate and mature processing conditions are not yet available to produce usable SOS wafers from as-grown state. A defect free and residual stress free SOS wafer is still unavailable. Lattice mismatch and difference in thermal expansion coefficients between silicon and sapphire materials are main causes of imperfections.

Characterization methods used for common/semiconductor materials can be used to SOS wafers. Because of its multilayered structure and very thin Si layer, special attention/techniques/accessories are normally required while applying these methods to SOS wafers. To date, the structural defects can be characterized qualitatively by TEM and X-ray topography. On the other hand, ion-channeling and X-ray rocking curve methods are capable of measuring these defects quantitatively. Average residual stresses can be measured nondestructively by Raman scattering with a high spatial resolution. The XRD technique can be used for residual stress analysis if a more complete stress tensor becomes necessary. The measurement of complete residual stress/strain tensors in a wafer surface and along the thickness of a thin film is still in an early stage of research and development.

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