Transient Thermal Analysis of Sapphire Wafers Subjected to Thermal Shocks

T. Vodenitcharova, L. C. Zhang, I. Zarudi, Y. Yin, H. Domyo, and T. Ho

***Abstract*—Rapid heating and cooling are commonly encountered events in integrated circuit processing, which produce thermal shocks and consequent thermal stresses in wafers. The present paper studies the heat transfer in sapphire wafers during a thermal shock as well as the dependence of the wafer temperature on various process parameters. A three-dimensional finite-element model of a single sapphire wafer was developed to analyze the transient heat conduction in conjunction with the heat radiation and heat convection on the wafer surfaces. A silicon wafer was also investigated, for comparison. It was found that the rapid thermal loading leads to a parabolic radial temperature distribution, which induces thermal stresses even if the wafer is not mechanically restrained. The study predicted that for sapphire wafers the maximum furnace temperature of 800 °C should be held for two hours in order to get a uniform temperature throughout the wafer.**

***Index Terms*—Sapphire, silicon, thermal shock, wafer.**

I. Introduction

SINGLE-CRYSTAL sapphire possesses some superior material properties, such as high strength, thermal conductivity and dielectric constant, excellent durability, and chemical stability. It is suitable for a large variety of products, ranging from windows, microwave plasma tubes, high-speed IC chips, silicon-on-sapphire (SOS) substrates, and dummy wafers [1]. Used as substrates/wafers in the semiconductor industry, sapphire often experiences thermal shocks during processing. For instance, these happen when the concentrically arranged wafers in a loading boat are inserted in a preheated furnace and when are taken out to the room temperature after processing. The thermal shocks lead to a considerable temperature variation, which may cause unexpected problems, such as fracture.

Experimental studies on silicon wafers subjected to rapid heating/cooling found that the axial temperature in the loading boat could vary up to 25 °C and the radial temperature up to 5 °C, at the maximum furnace temperature [2]. It was also reported that the introduction of shield rings at the end of the wafer stack reduces the edge-to-center temperature difference in the end wafers by around 3 °C [3]. It was claimed that radiation was the most important source of heat transfer inside a furnace and that conduction and convection through the gas in the furnace had a negligible effect. Nevertheless, conduction is the main factor of heat transfer within a single wafer.

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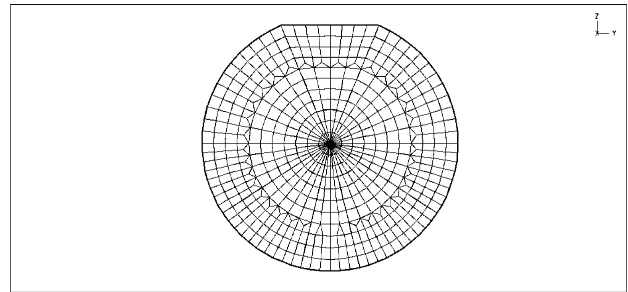

Fig. 1. FEA model in heat transfer simulations.

Since heat conduction is a transient process, it induces radial temperature variations across the wafer and can lead to high stresses and plastic deformations. Severe deformation patterns were observed, of a saddle-type on insertion and of a bowl-type on withdrawal [4], [5]. The phenomena on silicon wafers were theoretically modeled and the experimental observations were reasonably explained [3], [6]–[9]. Some authors believed that it was the temperature nonuniformity at the highest furnace temperature that stressed the wafer beyond its yield stress [3]. Some others, however, claimed that the most severe stresses occurred during the wafer withdrawal, which could result in dislocations or warping. Additionally, temperature nonuniformity causes mechanical stresses at the interface in silicon-on-insulator structures during fabrication and subsequent debonding [7].

Although the published literature provides deep insight into the temperature and stress developments during thermal shocks, it concentrates on silicon wafers only; there are no reports on sapphire wafers. It is therefore the purpose of this paper to study the temperature distribution in sapphire wafers exposed to thermal shocks.

II. FEA Model

The sapphire wafers having R-plane orientation are almost circular (150 mm in diameter and 0.6 mm thick) with a flat side; see Fig. 1.

The global coordinate system is defined as follows: X is perpendicular to the wafer face, Y is horizontal, and Z is vertical. The wafers are first loaded to a boat for processing. Upon insertion and withdrawal from a furnace, a wafer normally experiences a thermal cycle shown in Fig. 2. In some cases, according

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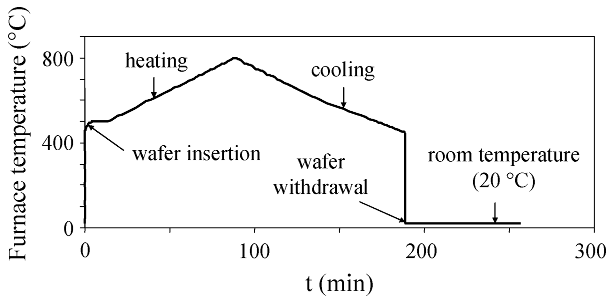

Fig. 2. Furnace temperature profile.

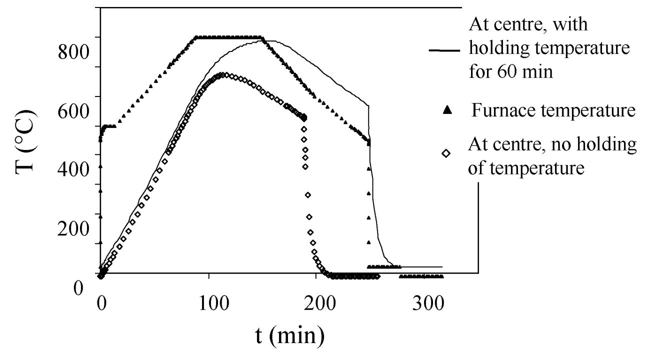

Fig. 3. Temperature at center of sapphire wafer T_{center} versus time t (for $\varepsilon_a = 0.7$).

to the current practice, the target temperature is held constant for 60 min.

The loading boat is assumed to have shields and dummy wafers at both ends, and the gap between two adjacent wafers is small (about 2 mm) which reduces the radiation effect of the furnace doors on the end wafers. Thus, the temperature variation along the furnace can be neglected at a first approximation, and all the wafers can be assumed as exposed to the same thermal conditions (being in thermal equilibrium). This allows us to study only a single wafer as a representative of a wafer batch. Furthermore, the first wafer in the batch is exposed to the high furnace temperature for a longer period than the others because of the way the loading boat travels in the furnace. For that reason, the finite-element analysis (FEA) is conducted on the first wafer only (note that the temperature profile in Fig. 2 is for the first wafer in the batch). It is further assumed that heat in the furnace transfers to the wafer mainly through radiation to the wafer edge. The heat transfer in the wafer is then by conduction. Since convection has a negligible effect during processing, it is activated only on the edges during insertion and withdrawal and on the front wafer face during withdrawal. Radiation is ignored after withdrawal from the furnace. The activation and deactivation of the radiation and convection elements is achieved by using the birth–death option in the FEA software, ADINA.

A transient heat conduction is carried out, with initial conditions. The wafer is modeled using linear three-dimensional (3-D) conduction elements, four-node boundary radiation elements, and four-node boundary convection elements on all surfaces; see Fig. 1.

The sapphire wafer thermal properties are considered temperature dependent and input as piecewise linear functions of the temperature: coefficient of thermal conductivity k $[W/(\mathrm{m}/K)] = 42$ at 291 K, 46 at 300 K, 32.4 at 400 K, 18.9 at 600 K, 13.0 at 800 K, and 10.5 at 1000 K [10]. The specific heat c_p (in Joules per kilogram Kelvin) is taken as 761 at 291 K, 765 at 300 K, 940 at 400 K, 1110 at 600 K 1180 at 800 K, and 1225 at 100 K [10]. The convection coefficient h $[W/(\mathrm{m}^2K)]$ is assumed 6.8 at 100 °C, 8.9 at 275 °C, and 10.0 at temperatures greater than 450 °C (for a free convection of a vertical plate and the properties of air as given in [10]). The density ρ is specified as 3970 kg/m^3 [10]. The coefficient of emissivity is taken as an effective emissivity ε_a, as introduced in [11], to count for the wafer–wafer and wafer–furnace radiation, where ε_a is a function of the cavity aspect ratio, i.e., the ratio of wafer radius to wafer spacing. This paper concentrates on sapphire substrates coated with a layer of silicon, which are used for fabricating SOS integrated devices. Although the optical properties of sapphire in the visible and near-infrared region is significantly different from that of silicon, its optical properties are similar to that of silicon beyond 1.1-μm wavelength. Silicon is transparent in the wavelength range between 1.1 and 9 μm, and sapphire is transparent in the wavelength range up to about 8 μm. The refractive index of sapphire is always lower than that of silicon in the entire wavelength range of thermal radiation. Therefore, in this paper, we take the emissivity of the sapphire wafers to cover the range of practical values of ε_a, namely 0.6, 0.7, 0.8, 0.9, and 1.0 for the reason of comparison with silicon [11]. The high emissivity of SOS and the small gap between two wafers allow us to consider thermal radiation as the main thermal loss mechanism in the furnace.

The simulations for the silicon wafer were run with the following properties [10]: $\rho = 2330$ kg/m^3; at temperature $T = 200\ K$: c_p [J/(kg K)] was taken as 556 and k [W/(m K)] as 264; respectively, at $T = 300\ K$: $c_p = 712$ and $K = 148$; at $T = 400\ K$: $c_p = 790$ and $K = 98.9$; at $T = 600\ K$: $c_p = 867$ and $K = 61.9$; at $T = 800\ K$: $c_p = 913$ and $K = 42.2$; and at $T = 1000\ K$: $c_p = 946$ and $K = 31.2$. ε_a is assumed to be 0.7, 0.8, 0.9 and 1 [11]. For h, we adopted the same values as for the sapphire wafer.

In the transient heat conduction analysis, five types of thermal loadings are imposed: 1) without holding the furnace temperature at the maximum temperature of 800 °C and 2) with holding the furnace temperature at 800 °C for 60, 70, 90, and 120 min, respectively.

III. Results

The transient heat conduction analysis shows that the wafer edge temperature T_{edge} lags the furnace temperature and that the center temperature T_{center} lags the edge temperature. Obviously, with time the wafer temperature gets closer to the furnace temperature; see Fig. 3. However, if after reaching the target of 800 °C, the furnace temperature is immediately decreased, as in Fig. 2, the wafer cannot reach the furnace temperature of 800 °C.

Some processes require temperature stabilization and the furnace temperature is held for $t_h = 60$ min at its maximum level of 800 °C in order to achieve temperature uniformity across the

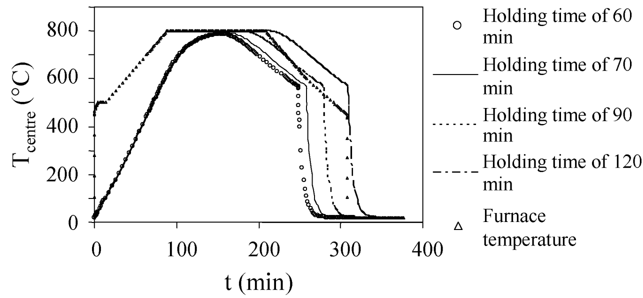

Fig. 4. Temperatures at center of sapphire wafer T_{center} versus time t for various holding periods t_h (for $\varepsilon_a = 0.7$).

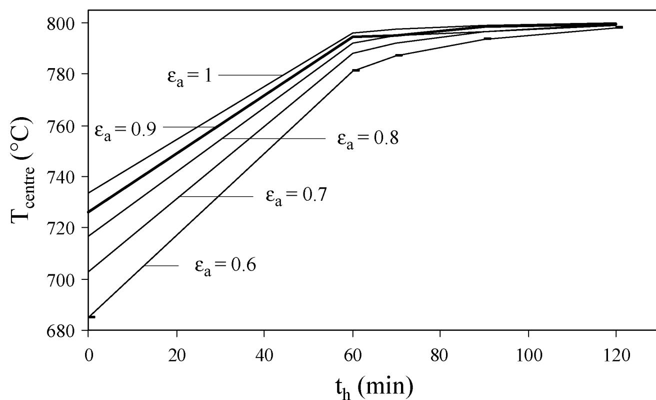

Fig. 5. Effect of holding time t_h on variation of temperature at center of sapphire wafer T_{center}.

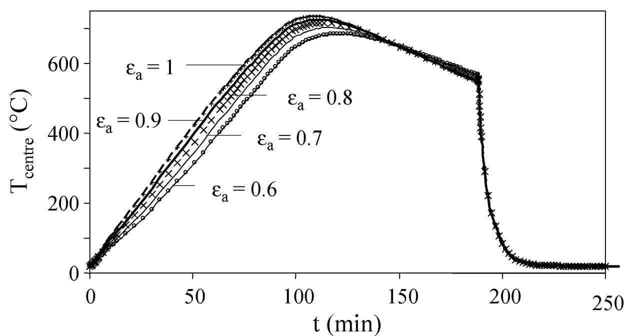

Fig. 6. Influence of coefficient of effective emissivity ε_a on variation of temperature at center of sapphire wafer T_{center} (no temperature holding).

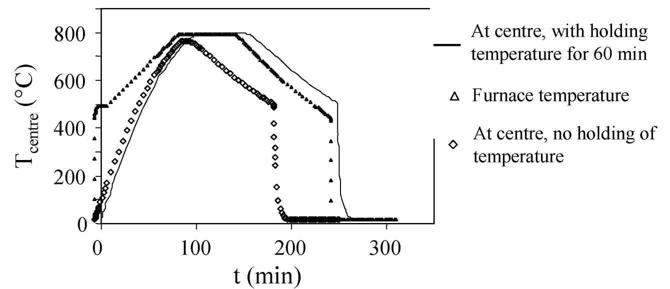

Fig. 7. Temperature at center of silicon wafer T_{center} versus time t ($\varepsilon_a = 0.7$).

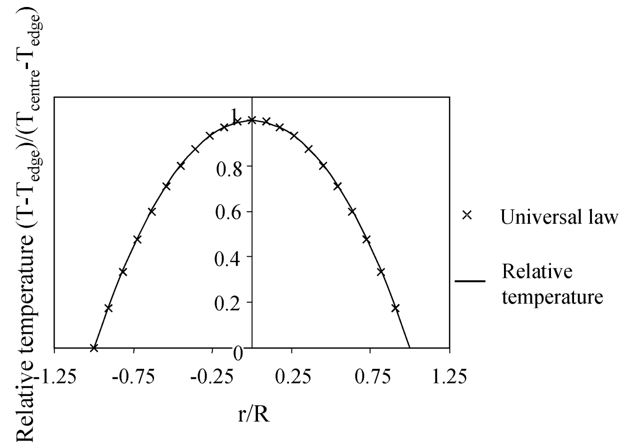

Fig. 8. Distribution of relative temperature $(T - T_{\text{edge}})/(T_{\text{center}} - T_{\text{edge}})$ in sapphire and silicon wafers along horizontal diameter at $T = 88.3$ min (for $\varepsilon_a = 0.7$); r denotes point location from center, and R is wafer radius.

wafer. This paper also considers holding times of 70, 90, and 120 min. It was observed that if the holding time t_h increases, the maximum wafer temperature at the center also increases; see Fig. 4. Figs. 5 and 6 illustrate the dependence of T_{center} on the coefficient of effective emissivity ε_a. T_{center} increases from 685.1 °C if $\varepsilon_a = 0.6$, to 733.6 °C if $\varepsilon_a = 1$ in the "no temperature stabilization" case and from 798.1 °C if $\varepsilon_a = 0.6$ to 799.85 °C if $\varepsilon_a = 1$ in the "120-min temperature holding" case.

The holding time that ensures that the furnace temperature of 800 °C will be uniformly distributed through the sapphire wafer (with an accuracy of 1 °C) depends also on ε_a. If $\varepsilon_a = 0.7$, the furnace temperature needs to be held for 119 min; if $\varepsilon_a = 0.8$, t_h decreases to 115 min; if $\varepsilon_a = 0.9$, t_h is 97 min, and for $\varepsilon_a = 1$, t_h is 88 min. For values of ε_a lower than 0.7, the wafer cannot reach the furnace temperature of 800 °C in this condition.

A comparison with the silicon wafer (for the practical values of ε_a from 0.7 to 1 [11]) shows that the silicon wafer follows the furnace temperature more closely; see Fig. 7. The temperature at the center T_{center} slightly increases with ε_a as it is 772 °C if $\varepsilon_a = 0.7$ and 780 °C if $\varepsilon_a = 1$, in the "no temperature holding" case. In the "with temperature holding" case the wafer center reaches the target temperature of 800 °C, for all values of ε_a, after the furnace has been held at 800 °C for 60 min.

It appears that the temperature distribution in both sapphire and silicon wafers is almost axisymmetric (except for the part near the flat edge of the wafer) and the temperature contour plots are almost concentric. The distribution of the temperature in the radial direction follows a parabolic law (Fig. 8), i.e., $(T - T_{\text{edge}})/(T_{\text{center}} - T_{\text{edge}}) = 1 = (r/R)^2$. The latter formula is known as the universal law. It is this nonuniform temperature distribution that induces thermal stresses and strains in the wafer.

Of great importance is the magnitude of the edge-to-center temperature difference $\Delta T = T_{\text{edge}} - T_{\text{center}}$. In the heating phase, ΔT is positive and initially increases steeply; see Fig. 9. Whereas, if the wafer is traveling within the furnace, ΔT is almost constant. In the ramping-up phase, it increases sharply again. Cooling the furnace decreases ΔT and eventually makes it zero, indicating that the wafer temperature becomes uniform throughout. It appears that ΔT in the "with temperature stabilization" cases drops slower than in the "no temperature stabi-

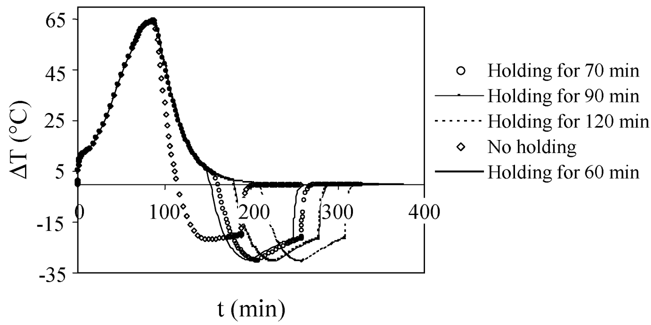

Fig. 9. Effect of temperature holding on variation of edge-to-center temperature difference ΔT in sapphire, with time t (for $\varepsilon_a = 0.7$).

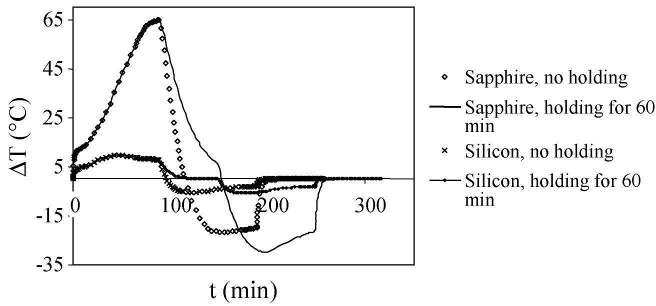

Fig. 10. Edge-to-center temperature difference ΔT versus time t (for $\varepsilon_a = 0.7$).

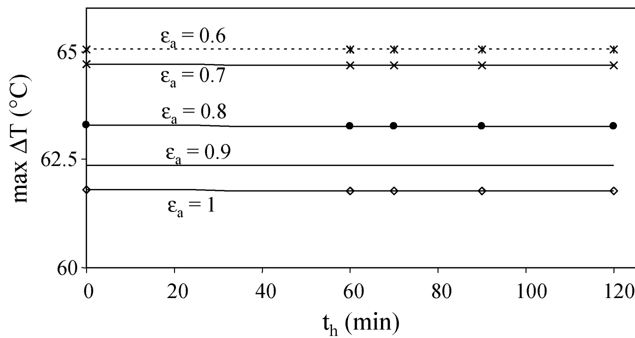

Fig. 11. Effect of temperature holding time t_h on maximum temperature difference ΔT in sapphire.

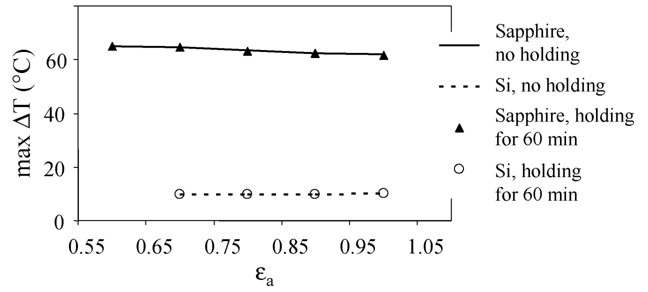

Fig. 12. Comparison between maximum temperature difference ΔT of sapphire and silicon wafers.

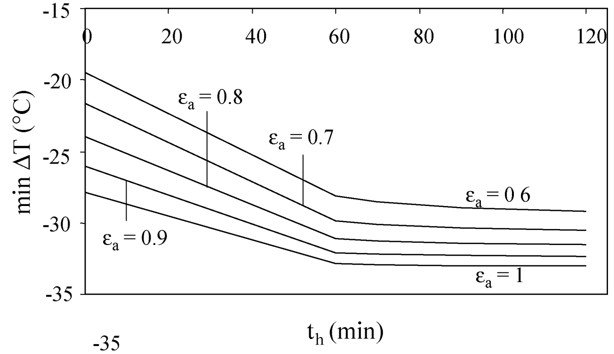

Fig. 13. Effect of effective emissivity ε_a and temperature stabilization on minimum temperature difference ΔT in sapphire wafers.

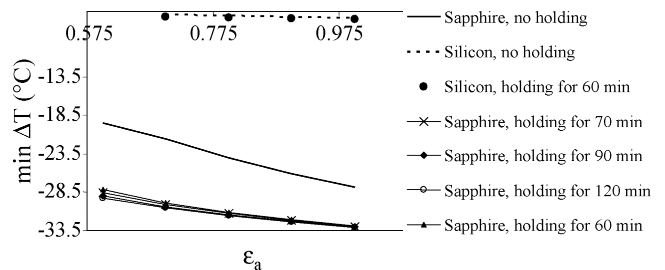

Fig. 14. Comparison between minimum temperature difference min ΔT of sapphire and silicon wafers.

lization" case, and its minimum value is larger. Further cooling makes ΔT negative, i.e., the wafer center becomes hotter than the wafer edge. Upon withdrawal, the wafer temperature decreases to the room temperature and ΔT becomes zero. The time needed to bring the wafer temperature to the room temperature is called cooling time t_c.

A comparison between a sapphire wafer and a silicon wafer shows that ΔT in the latter is smaller and reaches its maximum and minimum values much faster than in the former; see Fig. 10.

The contribution of the effective emissivity ε_a to the maximum ΔT appears to be negligible. If ε_a varies from 0.6 to 1 in sapphire wafers, the maximum ΔT in the case of 120 min temperature holding is 65.1 °C if $\varepsilon_a = 0.6$, 64.7 °C if $\varepsilon_a = 0.7$, 63.3 °C if $\varepsilon_a = 0.8$, 62.4 °C if $\varepsilon_a = 0.9$, and 61.8 °C if $\varepsilon_a = 1$; see Fig. 11. Furnace temperature holding has no effect on max ΔT for the values of ε_a considered. However, maximum ΔT in a silicon wafer is almost independent of ε_a being 9.7 °C if $\varepsilon_a = 0.7$ and 10.0 °C if $\varepsilon_a = 1$; see Fig. 12.

Nevertheless, increasing ε_a from 0.6 to 1 and temperature stabilization from 60 to 120 min increases the values of minimum ΔT, which in sapphire wafers is -19.5 °C to -27.8 °C in the "no temperature stabilization" case, -28.1 °C to -32.9 °C if $t_h = 60$ min, -28.5 °C to -32.9 °C if $t_h = 70$ min, -29.0 °C to -33.0 °C if $t_h = 90$ min, and -29.2 °C to -33.0 °C if $t_h = 120$ min; see Figs. 13 and 14.

Silicon wafers develop a smaller negative temperature difference i.e., -5.4 °C to -5.8 °C in the "no temperature stabilization" case, and -5.7 °C to -6.0 °C in the "60-min holding" case; see Fig. 14.

Another parameter of interest is t_u, the time needed to make the wafer temperature uniform after the target temperature is achieved, which is the same as the time at which the wafer center reaches its maximal value. A comparison between the results for sapphire wafers with various ε_a shows that t_u decreases if ε_a increases and increases if the furnace temperature is held; see

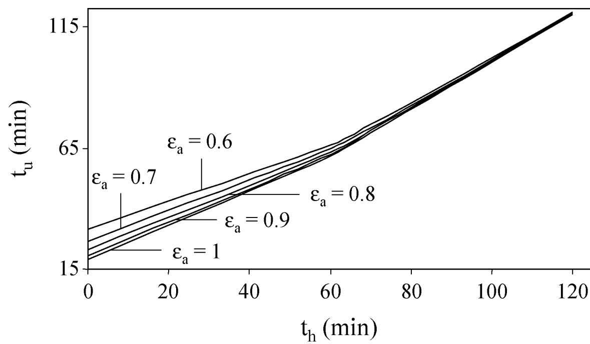

Fig. 15. Effect of effective emissivity ε_a and temperature stabilization on time for uniform temperature T_u in sapphire wafers.

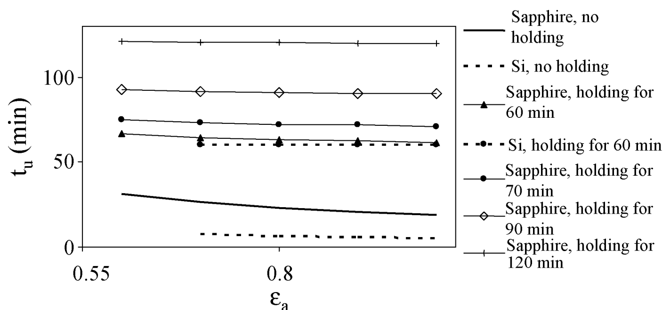

Fig. 16. Comparison between time T_u for uniform temperature of sapphire and silicon wafers, for varying coefficients of effective emissivity ε_a.

Figs. 15 and 16. In sapphire wafers, t_u varies between 31.5 min for $\varepsilon_a = 0.6$ to 18.8 min for $\varepsilon_a = 1$ in the "no temperature stabilization" case. However, since it happens in the ramping-down phase, the wafer temperature is significantly below the furnace temperature of 800 °C, i.e., around 685.1 °C if $\varepsilon_a = 0.6$ and increases to 733.3 °C if $\varepsilon_a = 1$; see Fig. 5. Temperature stabilization increases the wafer temperature, but again temperature uniformity is achieved in the ramping- down phase; therefore, the wafer has not had enough time to reach the furnace temperature. If the holding time is $t_h = 60$ min, the time for uniform temperature distribution t_u decreases from 66.5 min if $\varepsilon_a = 0.6$ to 61.7 min if $\varepsilon_a = 1$, in which case T_{center} increases from 781.4 °C to 795.8 °C, respectively. If the holding time $T_h = 70$ min, t_u decreases from 74.8 min if $\varepsilon_a = 0.6$ to 71.1 min if $\varepsilon_a = 1$, in which case T_{center} increases from 787.0 °C to 797.5 °C, respectively. If $t_h = 90$ min, t_u decreases from 92.7 min if $\varepsilon_a = 0.6$ to 90.5 min if $\varepsilon_a = 1$, in which case T_{center} increases from 793.8 °C to 799.1 °C, respectively. Finally, if $t_h = 120$ min, t_u is around 120 min for $\varepsilon_a > 0.6$, in which case T_{center} is 798.1 °C if $\varepsilon_a = 0.6$, and 799.8 °C if $\varepsilon_a = 1$. As already mentioned, achieving a uniform wafer temperature of more than 799 °C requires holding the furnace temperature from 120 to 88 min if ε_a varies from 0.7 to 1; for lower ε_a, the wafer temperature could not reach 800 °C. Obviously, the current practice of holding the temperature for 60 min, although sufficient for silicon wafers, does not ensure the target temperature of 800 °C in sapphire wafers and temperature uniformity.

In contrast, silicon wafers need much less temperature holding time for temperature uniformity; see Fig. 16. For the "no temperature stabilization" case, t_u decreases from 7.4 min if $\varepsilon_a = 0.7$, to 5.4 min if $\varepsilon_a = 1$. Holding the furnace temperature for 60 min is exactly what silicon wafers need in order to achieve the designed process parameters, i.e., uniform temperature of $T_{\text{center}} = 799.9$ °C across the wafer.

This paper also estimates the cooling time t_c needed to cool the wafer down to the room temperature of 20 °C upon withdrawal from the furnace. It was found that sapphire wafers need a longer time to cool down to a uniform temperature $T < 21$ °C, T_c being around 35 min (no matter whether temperature stabilization is present). For silicon wafers, t_c is around 20 min in all cases. Apparently, ε_a has almost no effect on t_c.

IV. Conclusion

This paper found that sapphire wafers need a longer furnace temperature holding time than silicon wafers in order to become uniformly heated at the target temperature (> 799 °C). While temperature holding of 60 min is sufficient for silicon wafers, sapphire wafers need as much as 2 h.

It was also discovered that during the thermal shock, the edge-to-center temperature drop ΔT developed in sapphire wafers is much larger than in silicon wafers, due to the sapphire's lower conductivity. For the process parameters in practice, it is evident that the largest value of ΔT is positive, max ΔT, and occurs at the point of the maximal furnace temperature. Upon cooling, ΔT decreases and becomes negative. Nevertheless, the largest value of the negative ΔT, min ΔT, is lower than max ΔT.

It became clear that a longer holding time for temperature stabilization will help achieve the uniform temperature distribution within a sapphire wafer at the target temperature of 800 °C, but on the other hand, it will increase min ΔT.

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